Single ended to differential MHEMT Transimpedance Amplifier with 66 dB-Ω differential Transimpedance and 50 GHz Bandwidth.

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Abstract — **In this paper, we demonstrate a single ended to differential transimpedance amplifier (TIA) with 66 dBΩ transimpedance gain, a 50 GHz 3-dB bandwidth and up to 700 mVp-p differential output voltage, fabricated in a 6-inch MHEMT process. The state-of-the-art gain-bandwidth product of this amplifier (>3THz), combined with its small chip size (1.9x1.1mm²), high sensitivity and low power consumption (<350mW) demonstrate the capabilities of a lumped MHEMT TIA design to realize a low cost receiver for 40Gb/s fiber optic communication systems.**

I. Introduction

Optical fiber communication systems require a sensitive receiver in order to maximize their reach. One of the key components in such receiver is the transimpedance amplifier, which interfaces the low current from the photodiode to the input amplifier of a clock and data recovery IC (CDR), which at 40 Gb/s is often realized in SiGe [1]. The input amplifier of the CDR is differential requiring a high-gain and low-noise TIA with DC-coupled differential output.

A significant effort has already spent to develop 40 Gb/s TIA's utilizing various InP, SiGe and GaAs process technologies [2-5] and either distributed or lumped circuit topologies. To achieve the best compromise between a moderate circuit size and the required gain performance, we have chosen to design a lumped transimpedance amplifier with 5 stages. To achieve sufficient bandwidth for such a lumped amplifier, the circuit was realized in a 6-inch 0.15μm metamorphic HEMT (M-HEMT) foundry technology. This technology achieves a transition frequency (f_T) of 120 GHz, and a maximum transconductance (g_m) of 700mS/mm.

II. CIRCUIT DESIGN

Figure 1 shows the schematic diagram of the circuit, which consists of a low-noise 3-stage single-ended transimpedance amplifier DC coupled to a 2-stage differential amplifier. Each stage is optimized to achieve the best compromise between gain and bandwidth. The high performance of the 0.15 μm M-HEMT, makes the high-frequency stability of a multi-stage design with high gain very critical. Due to the limitation of the models available in commercial simulators, we simulate the passive networks up to 150 GHz with an electromagnetic simulator to improve the design accuracy.

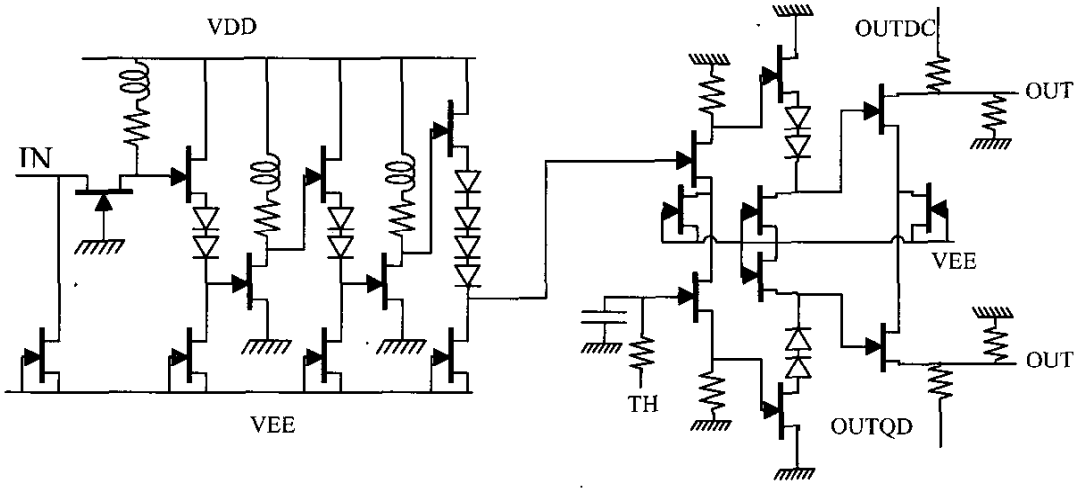

Fig. 1: Block diagram of the single-ended to differential transimpedance.

The TIA has +2V and –3V power supplies having a current consumption of 50mA and 40mA respectively.

The first stage is a common gate transistor to achieve good input return loss from DC to 50 GHz. The input admittance is approximately equal to,

$$Yin \approx (1+gm.Rd)/(Rd+Rl) + jCgs.\omega \quad (1)$$

$$If\ (Rd+Rl) >> Rd.Rl.Cds.\omega$$

with gm, Cgs, Cds, Rd and Rl respectively the transconductance, gate source capacitance, drain-source capacitance, drain-source resistance and load resistance. By selecting the transistor size and the resistive load, an impedance from 10 to 100 Ohm can be synthesized to optimize the interface between the photodiode and the transimpedance.

After the common-gate input stage a source follower with level-shifting diodes is used to transform the impedance and shift the DC level. A capacitor in parallel with the diodes reduces the losses at high frequencies and provides moderate gain peaking. The same topology is adopted after each common-source inverter (see figure 2). Short microstrip lines are used between the inverter and source follower and in series with the load to increase the bandwidth. A good compromise between transistor size, resistive load and the length of these series peaking lines allows sufficient gain and bandwidth.

After the 3-stage TIA, the signal is converted from single ended to differential. The slicing level can be set using a threshold offset control pin (THC), typically automatically adjusted such that the output DC offset voltage is cancelled. Finally, there are two differential stages, each consisting of a differential inverter preceded by one source follower.

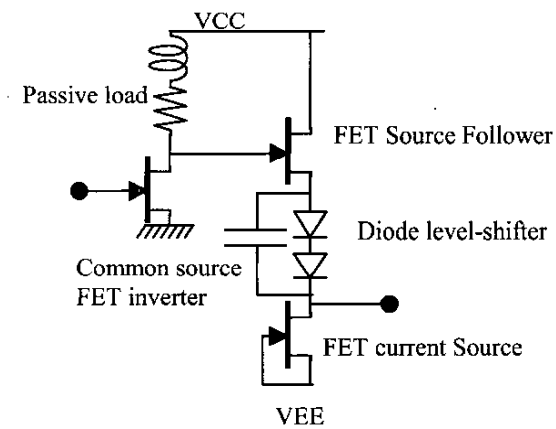

Fig. 2. Block diagram of the gain cell with peaked inductor passive load and capacitively by-passed diode

The last inverter is designed to achieve an output voltage swing adequate for the limiting input amplifier of the CDR and to be used either AC or DC-coupled. In the optimization of the return loss of the output stage the output bonding wire was taken into account, such that a low reflection is obtained after integration of the optical front-end module (OFE). A photograph of the transimpedance amplifier is shown below in Figure 3.

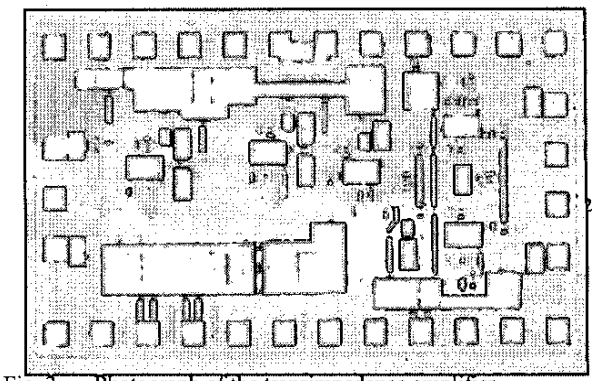

Fig. 3. Photograph of the transimpedance amplifier.

III. CIRCUIT RESULTS

The single-ended S-parameters, measured on-wafer with the unused output port terminated with a 50 Ohm load, are shown in figure 4. A very flat single-ended gain of 30 dB, or 36 dB differential gain, and a 3-dB bandwidth of 50 GHz are obtained. This translates in to a gain-bandwidth product of more than 3 THz, which is to our knowledge, the highest reported sofar for a TIA in any technology. Some ripple at the higher frequencies is caused by the difficult calibration of S-parameter measurements on such a high gain circuit The on-wafer measured output reflection S_{22} is less than –12 dB but is less than –15 dB when a 0.1 nH inductor is added to simulate the effect of short wire bonding (see black curve).

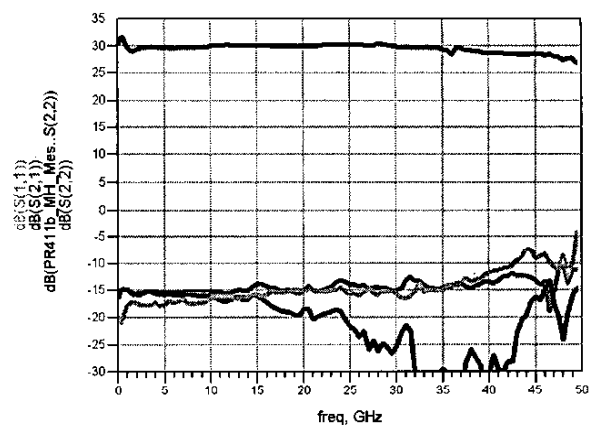

Fig. 4. Measured single-ended S-parameters on wafer.

Figure 5 shows the real and imaginary part of the input impedance of the TIA, as extracted from S-parameters. The real part is very constant as a function of frequency, which demonstrates the capabilities of the common gate topology to achieve flat impedance response up to very high frequencies. In our case, we obtained the desired value of 35 Ohm ± 5 Ohm up to 42 GHz.

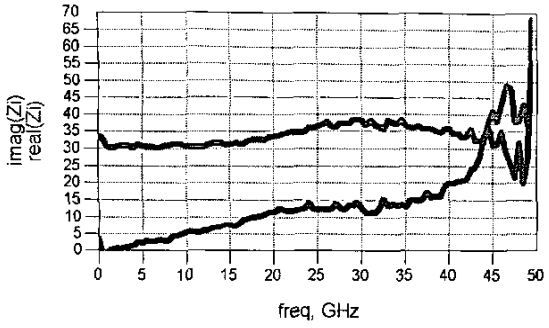

Fig. 5. Input impedance calculated from S-parameters.

Eye diagram measurements were performed on-wafer with DC-coupled output and a 40 Gb/s AC-coupled 2^{32}-1 PRBS input datastream. Connections between circuit and oscilloscope were kept minimal by using detachable samplers with high electrical bandwidth (70 GHz).

Figure 6 and 7 show both output signals when the TIA is respectively driven into its linear and limiting range. For a 7mVp-p input, a differential output signal amplitude of at least 200mV peak-to-peak is obtained, which is more then sufficient to drive the input limiting amplifier of the CDR. The quality of the output eye in the linear range is similar to that of an on-wafer measured through-line indicating the small amount of degradation caused by the TIA. The good eye quality for low input is also a good indication of the good sensitivity of this TIA. While the input referred current noise was not measured sofar, we expect a noise current below 25pA/sqrt(Hz) up to 40 GHz.

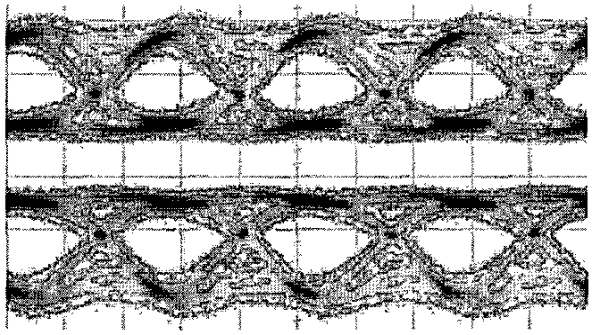

Fig. 6. Two outputs of the TIA driven with a $7mV_{pp}$ AC-coupled 2^{32}-1 40 Gb/s PRBS input datastream (scale:50mV/div).

When operating in the limiting range (figure 6), very open 40 Gb/s eyediagrams with a differential output swing of 700 mV_{pp} are obtained together with short rise and fall-times (<10 ps) and relatively low jitter (~5ps peak-to-peak).

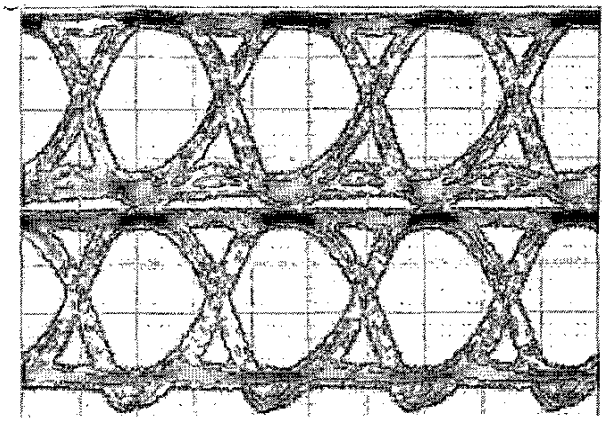

Fig. 7. Two outputs of the TIA driven with $70mV_{pp}$ AC-coupled 2^{32}-1 40 Gb/s PRBS input data (scale:100mV/div).

III. CONCLUSION

We have demonstrated a very compact, high gain, high bandwidth and low power consumption 40 Gb/s TIA fabricated in a 6-inch M-HEMT foundry process. The bandwidth of 50 GHz is comparable to that reported for lumped element InP or SiGe TIAs [2-4]. The gain-bandwidth product of more than 3 THz is, to our best knowledge, the highest reported sofar for any TIA [5]. This TIA monolithically integrates the single-ended to differential converter which simplifies module integration.

Input current noise measurements are under way and will be given during the presentation

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